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Low-noise custom VLSI for CdZnTe pixel detectors

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ABSTRACT

A custom analog VLSI chip is being developed for the readout of pixellated CdZnTe detectors in the focal plane of an astronomical hard X-ray telescope. The chip is intended for indium bump bonding to a pixel detector having pitch near 0.5 mm. A complete precision analog signal processing chain, including charge sensitive preamplifier, shaping amplifiers and peak detect and hold circuit, is provided for each pixel. Here we describe the circuitry and discuss the performance of a functional prototype fabricated in a 1.2 μ m CMOS process at Orbit Semiconductor. Dynamic performance is found to be close to SPICE model predictions over a self-triggering range extending from 1 to 150 keV (200 to 30000 electrons). Integral non-linearity (1%) and noise (0.25 keV or 50 electrons FWHM with 200 fF input capacitance) while acceptable are not as good as predicted. Power consumption is only 250 μ W per pixel. Layout and design techniques are discussed which permit successful self-triggering operation at the low 1 keV threshold.

Keywords: x-ray astrophysics electronics CdZnTe

1. INTRODUCTION

In recent years the technology of multilayer reflectors has advanced sufficiently that astronomical focusing hard x-ray telescopes are feasible for energies up to near 100 keV. The first focusing hard x-ray telescopes are now being developed as balloon-borne payloads (HEFT¹ and InFocus²) and the technology is being readied for the Constellation space mission. The work described in this paper has been part of a program to produce a practical focal plane detector system for the HEFT (High Energy Focusing Telescope) payload and a prototype system for Constellation.

A focal plane detector system for the new focusing hard x-ray telescopes needs good detection efficiency and position resolution, yet only modest area. Typical requirements are for position resolution of 0.5 mm over a 2.5 by 2.5 cm detector area. Position-sensitive CdZnTe detectors can meet these requirements and also offer good energy resolution, near room temperature operation, and solid-state reliability. The basic capability of position-sensitive CdZnTe detectors has been demonstrated using both pixellated³ and orthogonal-strip⁴ contact geometries. Early in our study we noticed the potential of the pixellated contact geometry to yield excellent energy resolution. Electronic noise could be very low due to small pixel capacitance and leakage current, while the detrimental affect of signal induced by trapped holes could be minimized. However, existing readout chips for pixellated detectors were of the "multiplexer" type³, in which the signal is integrated passively in all pixels then readout sequentially in a scanning operation. Due to the typically long integration times (milliseconds) the energy resolution is limited by leakage current shot noise. In addition, a prompt signal is not available for each hard x-ray event for use with an anti-coincidence shield.

Using the tools and experience gained during the successful development of two custom analog VLSI chips⁵ for NASA's Advanced Composition Explorer mission, we are developing a new readout chip intended for indium bump bonding to a CdZnTe pixel detector. Each pixel is to be read out by a self-triggering signal processing chain that includes a charge-sensitive preamplifier, shaping amplifiers, and a peak detect/hold circuit. The circuit design, layout and performance of a prototype chip are discussed below. This prototype chip has achieved very low noise operation and supplies a prompt signal (suitable for operation with an anti-coincidence shield) over a dynamic range corresponding to 1-150 keV energy loss in CdZnTe. However, this prototype chip was not intended for bonding to a detector, but rather has an on-chip capacitor and leakage current source for electronic simulation of a detector pixel. Plans for a second prototype chip, which will be bonded to a detector, are also discussed below.

2. READOUT DESIGN

Design choices were influenced by several considerations. The desire for low electronic noise and self-triggering capability down to a noise limit near 1 keV suggested the use of continuous-time shaping and peak detection, and argued against the use of continuously running clock signals. The desire to operate the CdZnTe detector slightly cooled (to about 0 degree C) to reduce leakage current placed a premium on low power operation. The low expected count rate of <100c/s for even the brightest x-ray sources together with the low leakage current derived from fine pixels and moderate cooling implied relatively long optimum signal shaping time constants. The available area below each pixel of about 0.5 by 0.5 mm required a compact design but allowed enough room for the sophistication needed to achieve good linearity and stability which will be desired when summing spectra over numerous pixels and long observing times. The desire for low cost prototyping and high density led to the choice of Orbit's 1.2 μm double-poly double-metal CMOS process.

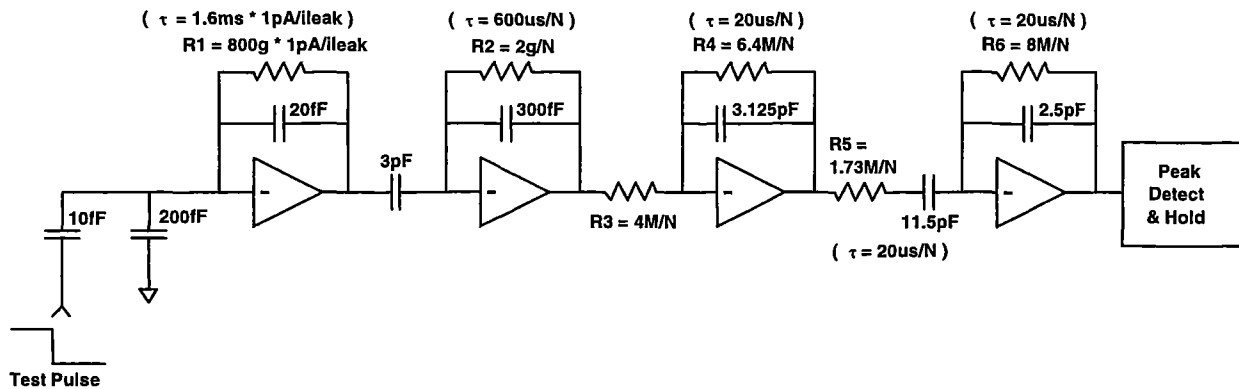


Figure 1: Simplified pulse processing chain

A simplified schematic of the pulse processing chain for a single pixel is shown in Figure 1. Signal amplification occurs in the first two low-noise preamplifier stages, boosting full-scale signals to amplitudes near 3 Volts. The long restoration time constants in these stages are required for low noise operation and were implemented using large resistances simulated with active circuitry described below. Shaping of the signal for optimum noise performance occurs in the following two stages and yields an approximate pulse shape of $(t/\tau)^2 \exp(-t/\tau)$, with peak time of 2τ . The large resistances in the shaping section were also implemented with active circuitry and were designed such that the peak time can be digitally set over the range 5 to 40 usec. The peak detect/hold circuitry includes a comparator and the minimum logic needed to detect and hold the signal peak for off-chip analog to digital conversion.

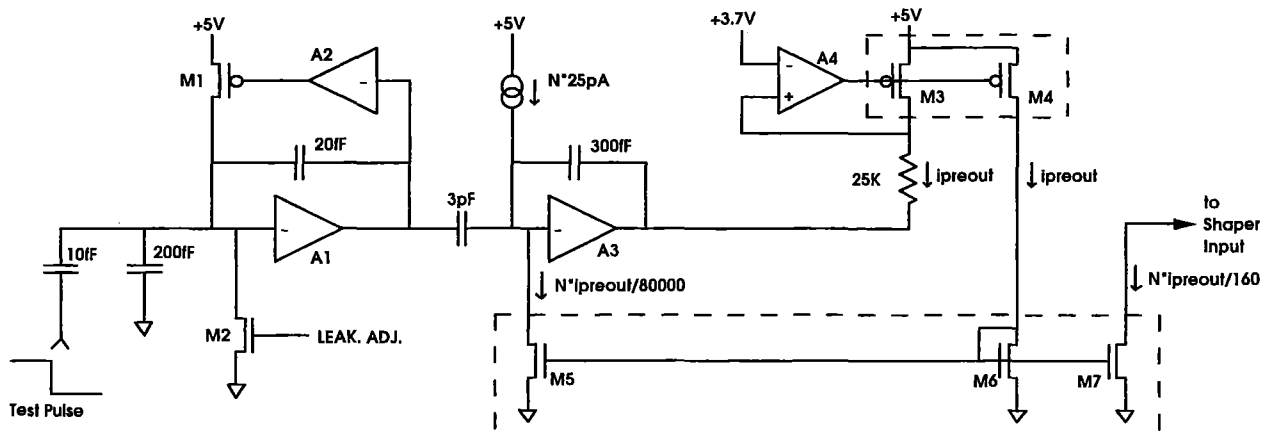


Figure 2: Preamplifier Section

More detailed schematics of the pulse processing chain are shown in Figures 2, 3 and 4. The preamplifiers, A1 and A3, shown in Figure 2 are of the folded cascode type, with the input amplifier A1 designed for use with a low pixel capacitance near 200 fF. The pmos input transistor has width 48 μm and length 1.8 μm , and is biased at a drain current near 3 μA . The very large effective resistance needed in the feedback loop of A1 is obtained using a pmos transistor, M1, of length 96 μm and width 1.8 μm , biased sub-threshold by amplifier A2 having gain $\frac{1}{2}$. The detector leakage current is simulated with a current source represented by M2, while the detector capacitance is simulated by a 200fF on-chip capacitor. The design accommodates leakage currents in the range 0.1 – 10 pA, with the effective feedback resistance varying as a function of the leakage current as indicated in Figure 1. The variation of the feedback resistance is intentional and provides low noise operation for leakage currents near 0.1 pA (such as are expected with moderate cooling) but avoids DC saturation at the higher leakage currents near 10 pA (expected at room temperature). The effect of the non-linearity of this first stage feedback resistance on overall pulse response linearity is negligible since the output pulse amplitude is insensitive to the exact value of the long first stage decay time constant.

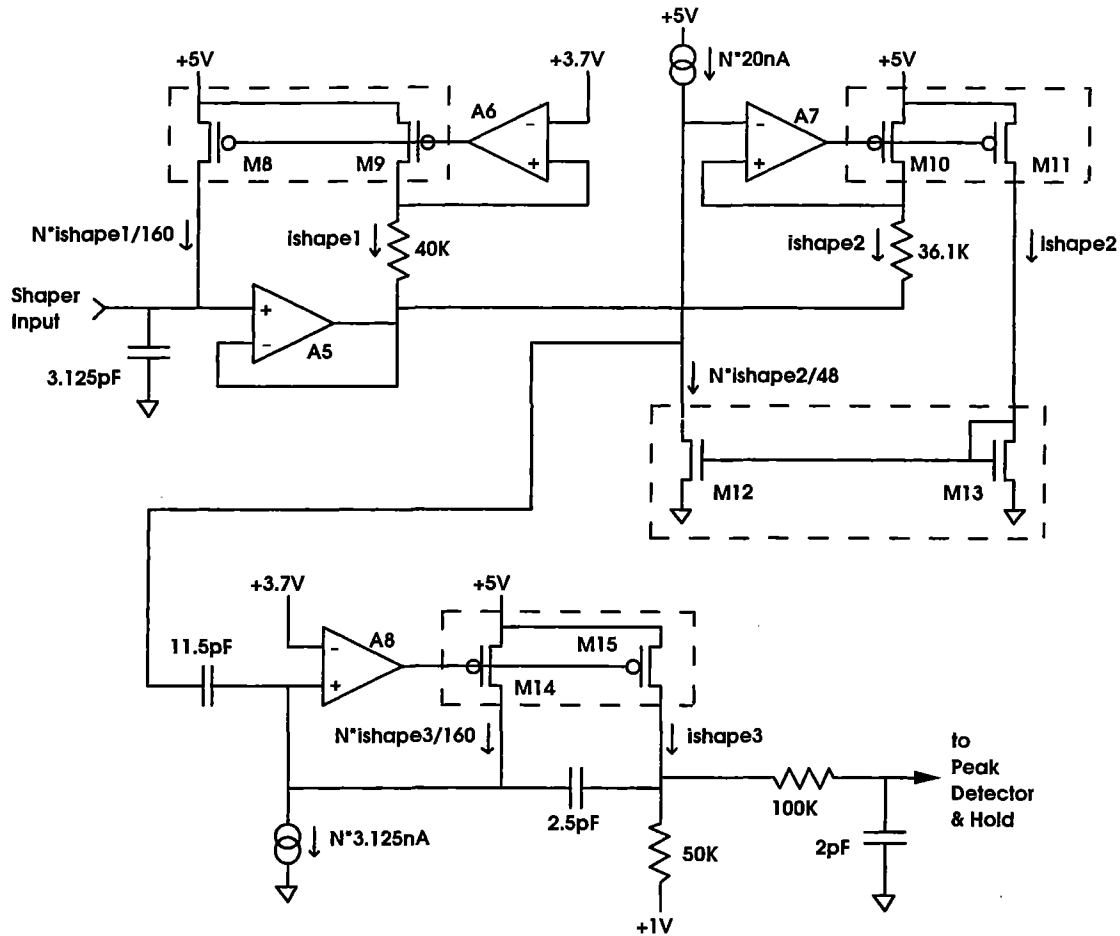


Figure 3: Shaping Section

A large effective resistance is also needed in the feedback loop of the second stage amplifier, A3, however in this case linearity is important since the decay time constant is closer in value to the shaping time constant. This feedback resistance, R2 in Figure 1, as well as other resistances R3 through R6, are implemented, as illustrated in Figures 2 and 3, using the combination of a smaller value polysilicon resistor, a current divider, and an amplifier. For example, the 2 giga-ohm resistance R2 of Figure 1 is implemented using a 25K polysilicon resistor working together with amplifier A4 and current mirrors/dividers represented by M3, M4, M5 and M6. The amplifier A4 holds one side of the 25K resistor at 3.7 Volts, converting the voltage signal at the output of A3 to the current signal labeled "ipreout". This current signal is divided by 80,000 for injection at the input of A3, implementing the desired effective feedback resistance of $80,000 \times 25\text{K}$ or 2 giga-

ohm. The “ipreout” current signal is also divided by 160 and injected into the shaping section, effectively implementing the resistance R3 of Figure 1. The current dividers represented schematically in Figures 2 and 3 (e.g. M5, M6, and M7) are actually implemented with sequences of dividers which alternate between nmos and pmos transistor sections, with each section performing division by an integer factor in the range 2 to 10. Each divider section employs cascoded current mirrors arranged such that the nominal division ratio is given by the relative numbers of identically sized and shaped input and output transistors. Care was taken in the design to ensure that the response time of the current divider chains is short compared to the shaping time constant and that the current division ratios are independent of the magnitude of the current. The effective values of the resistances R2 through R6 are programmable by switches in the current dividers that can be set to alter the division ratios. These switches are arranged to allow the variable N of Figure 1 to be set to 8, 4, 8/3, 2, 3/2 or 1, to obtain peak times of 5, 10, 15, 20, 30 and 40 usec respectively.

Figure 4: Peak Detect/Hold Section

feedback loop around A9 closes and the voltage on the hold capacitor again tracks the noise at the peak detector input. The "reset" signal is then removed and the system re-enters the quiescent state, ready for the next trigger.

Each pixel cell contains nine coupled amplifiers, each operating with somewhat different feedback and load. The amplifiers were kept as similar as practical to minimize the design effort. The non-differential amplifiers A1 and A3 are similar, as are the differential amplifiers A4 through A9. Low power operation with stable, high performance was achieved by tailoring the loop gain and phase versus frequency of each of these amplifiers as follows: The frequency (f_c) at which loop gain dropped to unity was positioned near 1 MHz, with phase margin typically between 45 and 60 degrees. Loop gain as a function of frequency, f , was tailored to vary as $1/f$ between 250 kHz and 1 MHz. For frequencies below 250 kHz, the dependence was steepened (often using internal positive feedback) to obtain high loop gains at frequencies in the pass band of the shaping section. Typical loop gains were 150 and 3000 at 45 and 5.6 kHz (the center frequencies of the shaping section pass band for 5 and 40 usec peak time settings respectively) and are compatible with our goal of integral non-linearity of less than about 0.1%.

Amplifiers were designed and compensated to ensure that loop gain characteristics were approximately independent of output current and slew rate over the expected operating range. This effort was particularly important for amplifier A9 of the peak detect/hold circuit since the drain current of output transistor M17 varies over a wide range from the 30 nA standing current to the maximum hold capacitor charging current near 70 μ A. Without compensation, the large variation in transconductance induced in M17 could cause a dramatic and undesirable shift of f_c toward higher frequency during heavy charging of the hold capacitor, leading to oscillation. The compensation methods employed here, as well as the architecture, are similar to those used in discrete and VLSI bipolar pulse processing chains designed for precision low-power space applications over the past 30 years.^{5,6,7}

The layout of the pulse processing chain was critical since all circuitry within a pixel cell must lie in close proximity to the sensitive preamplifier input node. The desired low noise and triggering threshold was obtained (at least in the prototype chip with no detector yet coupled!) using the following layout and design guidelines:

- 1) No on-chip digital signal transitions were permitted during the quiescent state (i.e. while awaiting an x-ray event).
- 2) During the critical time between the occurrence of an x-ray event and the associated peak detection/hold, no on-chip digital signal transitions were allowed, except those occurring locally within a pixel and associated with the peak detection itself.
- 3) The preamplifier input (a metal 2 contact) was shielded from the substrate using a grounded metal 1 layer and numerous connections to the substrate in the vicinity of the input were made to this grounded shield.
- 4) All circuitry (except, of course, the preamplifier itself) was kept as far away as possible from the preamplifier input.
- 5) All DC power and bias voltage buses were run in parallel across the pixel cell using the metal 2 layer to effectively cover the cell circuitry with a shield intended to reduce stray capacitance from the circuitry to the preamplifier input.
- 6) Three separate power and ground bus pairs were required: One for the digital circuitry, one for the bulk of the analog circuitry and one used only for the preamplifiers.
- 7) The power and ground buses (as well as the current carrying 1V bus which supplies a reference level at the peak detector input) were made as wide as possible and connected both horizontally and vertically to minimize noise due to variations in supply currents during pulse processing.
- 8) A separate pathway was provided between pixels for the digital signals (needed to communicate peak detection from the pixels to peripheral logic and to control and reset the circuitry within pixel cells.) These digital signals were run using metal 2 and were shielded from the substrate with a grounded layer of metal 1.

The layout for a single pixel cell resulting from these guidelines is shown in Figure 5. The sensitive preamplifier input is located in the center of the cell, with the preamplifier located immediately below. The amplification chain spirals around the pixel contact in a counter-clockwise direction ending with the peak detector/hold circuitry located in the lower left corner. DC power and bias voltage lines run horizontally and largely cover the cell with a metal 2 layer as mentioned in 5) above. The digital signal pathway mentioned in 7) runs horizontally across the bottom of the cell. The dimensions of the pixel cell shown in Figure 6 are approximately 670 by 650 μ m. This is larger than our goal of 500 by 500 μ m partly due to the extra layout space needed to implement programmable peak times.

The proto-type chip design included four pixel cells. One cell was instrumented with eight test points which could be connected one at a time (via an on-chip analog multiplexer) to an on-chip precision unity gain buffer amplifier having bandwidth near 10 MHz (significantly higher than the 1MHz loop bandwidths of the pixel cell amplifiers). The buffer amplifier output was routed to a bond pad and was designed to drive an oscilloscope probe for precision viewing of the test point signals. The on-chip analog multiplexer used to select the test point could also be set to connect another bond pad to the buffer amplifier input for stimulation and verification of the amplifier's response characteristics.

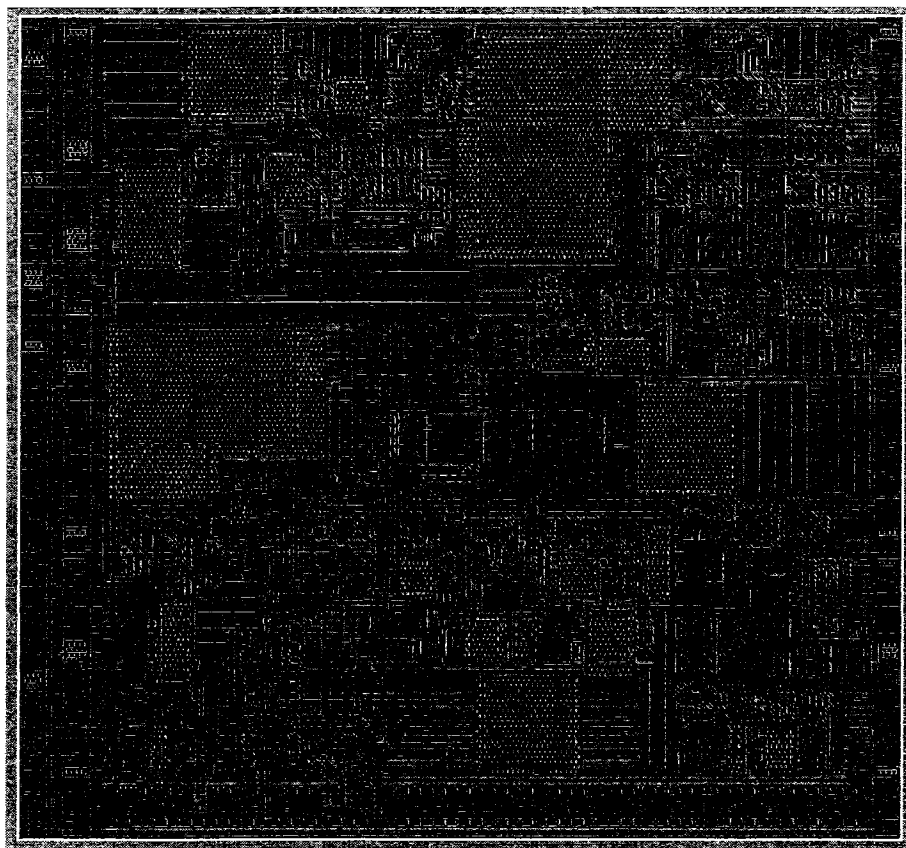


Figure 5: Layout of one pixel cell

The layout was performed using MAGIC version 6.4.5, available in the public domain. All circuit designs were extensively simulated with Cadence SPICE and level 3 MOS transistor models, in the context of the Cadence Analog Artist design system. Layout versus schematic consistency checking was done using the publicly available Gemini program.

3. PERFORMANCE

In spite of the use of the Gemini program to check layout versus schematic consistency, the prototype chip was discovered to have a layout error in the shaping section. (This layout error went undetected because our automated check process failed to properly account for poly-silicon resistors.) An attempt was made to repair a few chips using micro-machining techniques. The repair was successful only on one chip for the pixel cell having test points extracted. Thus one completely functional pulse processing chain was obtained and tested.

The dynamic performance of the various amplifiers was found to be as expected. The on-chip buffer amplifier performed well, allowing the signals at various test points to be viewed with an oscilloscope. The impulse-response of the preamplifier stages, and the error signals for amplifiers in subsequent stages were close in shape and amplitude to SPICE predictions. The shape of the signal at the input to the peak detector was also correct, with the settable time to peak in agreement with the nominal 5, 10, 15, 20, 30 and 40 usec values within a few percent. This agreement (which was better than process variations would usually allow) was possible given that the capacitance per unit capacitor area and the sheet resistance of the polysilicon happened to be close to their nominal values for the particular wafer from which the prototype chip was extracted. In addition, the good agreement of peak times also indicated that the current dividers used in the simulation of the large resistances in the shaping networks were performing close to expectations. The peak detect/hold circuitry also appeared to function properly over the full dynamic range from about 1 to 150 keV. The reset sequence could be performed successfully without retriggering. Inspection of the various test points with an oscilloscope indicated that any perturbations due to digital signal transitions were considerably smaller in amplitude than the thermal noise.

Detailed measurements of the impulse transfer function showed a much larger than expected integral non-linearity of about 1%. (SPICE simulations had indicated about 0.1% maximum deviation from a straight-line fit to the transfer function as a percentage of full scale.) This non-linearity was tracked to the shaping section of the signal processing chain and is apparently due to imperfection in the current dividers. The prototype chip contains copies of the current dividers as individually accessible test structures. Non-linearities in these current divider test structures were found to be similar in magnitude and shape to the non-linearity found in the overall pulse chain transfer function.

The noise performance of the pulse processing chain was acceptable, but not as good as SPICE predictions. For the 40 usec peak time setting and simulated detector leakage near 0.1 pA the measured noise referred to the input was equivalent to approximately 0.25 keV FWHM (or about 50 electrons) energy loss in CdZnTe and was a factor of two higher than SPICE predictions. Investigation of the cause of the discrepancy continues. Since noise measurements are available for all peak time settings and a wide range of simulated detector leakage currents, we expect to be able to isolate the cause. One likely possibility is that the flicker noise coefficients for the pmos and nmos transistors used in the SPICE simulations are not representative for the particular prototype chip we have investigated. Test structures on the chip will allow direct measurement of these coefficients, which has yet to be done.

The noise performance was degraded an additional factor of two for signals near threshold in the range 1 to 5 keV. This degradation was traced to noise in the peak detection circuit, which caused a pulse to pulse variation in the sensed peak time for low amplitude signals. In addition, the DC offset of the comparator in the peak detection circuit was unacceptably large, also degrading performance for low level signals. Thus, the peak detector has been partly redesigned. The internal noise has been reduced to an acceptable level and an auto-zeroing capability has been designed into the comparator.

4. FUTURE DEVELOPMENT

Given the mostly successful operation of the first prototype chip discussed above we proceeded with the design of a second prototype chip intended for indium bump bonding to a CdZnTe detector. The design, layout and submission for fabrication of this chip has been recently completed. The only modification to the signal processing chain was the improvement of the peak detector mentioned above. This second prototype contains an 8 by 8 array of pixel cells and includes the additional logic to locate and route stored peak voltages for off-chip analog to digital conversion. The chip contains additional diagnostic capability. All eight of the pixel cells along one outer column are instrumented with accessible test points routable to an on-chip oscilloscope buffer amplifier. The delivery of test signals to the various pixels is programmable to allow the characterization of pixel to pixel cross-talk. The preamplifier output from any of the 64 pixels can be routed to a bond pad allowing its DC voltage to be measured as a diagnostic indicator of pixel leakage current.

A third prototype chip is in the planning stage. The goal will be to reduce the size of the pixel cell to 0.5 by 0.5 mm or smaller. As mentioned earlier this goal will be achieved in part by removing the programmability of shaping peak time, which was implemented as a tool for the study of CdZnTe pixel detectors and will not be needed in a future hard x-ray telescope application. We are also likely to design the third prototype chip for a CMOS process incorporating high resistivity poly-silicon (available at Orbit and Mitel, for example). This will simplify the design, lower power consumption, and improve linearity of the shaping section since active current dividers will not be needed to implement the shaping network resistances.

5. ACKNOWLEDGEMENTS

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